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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,957	08/21/2003	Arnold M. Frisch	CRED 2779	3002

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2138	

DATE MAILED: 04/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,957	FRISCH, ARNOLD M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 2/7/2006 has been reviewed.

2. Amendment filed on 2/7/2006 has been entered.

3. Applicant's arguments filed on 2/7/2006 have been fully considered but they are not persuasive.

4. The applicant contends, "As per claim 1, Dinteman's programmable delay circuit delays one timing signal TD to produce another timing signal TD' and does not directly produce a test signal supplied to an IC under test."

The examiner disagrees and would like to point out that Dinteman teaches that event phase modulator 46 includes a first-in, first-out (FIFO) buffer 52, a programmable delay circuit 54, and a programmable pattern generator 56. The indicating signal D is applied to a data input (DI) of FIFO buffer 52 while the timing signal TD is applied to a shift-in (SI) input of FIFO buffer 52. In response to each pulse of the timing signal TD, FIFO buffer 52 stores a control bit representing the current state of indicating signal D. Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52. Pattern generator 56 sets the DELAY data value provided to delay circuit 54 after each pulse of timing signal TD in accordance with a pattern defined by programming data provided as input to pattern generator 56 via computer bus 16. In response to each pulse of delayed timing signal TD', FIFO buffer 52 shifts its longest stored control bit onto a data-out terminal (DO) as the DRIVE signal provided to drive circuit 40 of FIG. 4 (fig. 4, 6, col. 6, lines 32-51, Dinteman). Thus programmable delay circuit provides a delayed timing signal TD', which is used to output signal from the buffer.

5. The applicant contends, "As per claims 2-3, one of skill in the art would not be motivated to use Churchill's programmable delay circuit to produce a jittery test signal for use in jitter testing because the scan bus could not supply data to frequency modulate input signal at a sufficient rate during a test when the IC is processing the jittery test signal."

The examiner disagrees and would like to mention that Dinteman teaches programmable delay circuit (fig. 6, Dinteman). Churchill only teaches that a programmable delay circuit can be within the IC (fig. 3, col. 20, lines 28-31, Churchill et al.).

6. The applicant contends, "As per claim 4, one of skill in the art would not be motivated to embed Dinteman's pattern generator in the IC under test since it would render Dinteman's test circuit non-functional."

The examiner disagrees and would like to point out that Adams et al. teaches an ABIST circuit on an integrated circuit including a programmable pattern generator (fig. 1, col. 3, lines 31-33, Adams et al.).

7. The applicant contends, "As per claims 5-6, Osawa provides no motivation for one of skill in the art to use Osawa's selector in connection with Dinteman's jitter generator circuit."

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Dinteman teaches that in decoding the incoming VECTOR, decoder 62 signals a set of four multiplexers 76 (fig. 8, col. 7, lines 28-29, Dinteman). Osawa et al. teaches selector circuit 233 (fig. 1, col. 33, lines 57-67, Osawa et al.). Thus Dinteman provides motivation to use Osawa's selector in connection with Dinteman's jitter generator circuit.

8. The applicant contends, "As per claim 7, a test signal is controlling Takatsuka's selector and is not one of the input signals that the selector is selecting, as in claim 7."

The examiner disagrees and would like to mention that Takatsuka et al. teach a selector circuit for receiving the second delay signal and the timing test signal, outputting the second delay signal in the normal mode, and outputting the timing test signal in the test mode (col. 12, lines 5-8, Takatsuka et al.).

9. The applicant contends, "As per claims 8-9, nothing in Bhawmik indicates that such an internally generated test signal should be applied as input to a programmable delay circuit within the IC which adds a controlled amount of jitter to the test signal."

The examiner disagrees and would like to mention that Dinteman teaches input to a programmable delay circuit within the IC, which adds a controlled amount of jitter to the signal (fig. 6, col. 6, lines 32-51, Dinteman). Bhawmik et al. teach a third means residing within the IC for generating the first signal and monitoring an output signal of the subcircuit (col. 1, lines 16-23, Bhawmik et al.).

10. The applicant contends, "As per claims 10-12, nothing in any of the cited sections of Dinteman mentions anything about any signal output of a delay circuit that can be fed back to the delay circuit's input so that the signal oscillates with a period that is a function of the delay of the delay circuit as recited in claims 10 and 11."

The examiner disagrees and would like to point out that Chetlur et al. teach a tester comprising a voltage controlled oscillator for generating a controllable frequency oscillating test signal (col. 6, lines 14-15, Chetlur et al.). Chetlur et al. also teach that the multiplexer supplies the test signal as the first signal input (fig. 1, col. 6, lines 22-24, Chetlur et al.).

Dinteman teaches a delay circuit (fig. 6, Dinteman). Dinteman also teaches that driver circuit 40 can produce a TEST signal that is a phase modulated version of the TEST signal defined by the input VECTOR data sequence, with the nature of the phase modulation being determined by the programming data inputs to event phase modulators 46 and 48 (col. 5, lines 51-56, Dinteman).

11. The applicant contends, " As per claim 13, one of skill in the art would not be motivated to use Churchill's programmable delay circuit 302 to produce a jittery test signal because it is controlled by data supplied by a scan bus."

The examiner disagrees and would like to mention that Dinteman teaches programmable delay circuit (fig. 6, Dinteman). Churchill only teaches that a programmable delay circuit can be within the IC (fig. 3, col. 20, lines 28-31, Churchill et al.).

The applicant also contends, "One of skill in the art would not be motivated to embed Dinteman's pattern generator in the IC under test since it would render Dinteman's test circuit non-functional."

The examiner disagrees and would like to point out that Adams et al. teaches an ABIST circuit on an integrated circuit including a programmable pattern generator (fig. 1, col. 3, lines 31-33, Adams et al.).

12. The applicant contends, "As per claim 14, nothing in Bhawmik indicates that an internally generated test signal should be applied as input to a programmable delay circuit."
Bhawmik et al. teach the third means residing within the IC for generating data (col. 1, lines 21-23, Bhawmik et al.).
Dinteman teaches a programmable delay circuit (fig. 6, Dinteman).

13. The applicant contends, "As per claim 22, the output signal TD' of Dinteman's programmable delay circuit is not a jittery test signal supplied as input to a subcircuit of an IC under test."
The examiner disagrees and would like to point out that Dinteman teaches that event phase modulator 46 includes a first-in, first-out (FIFO) buffer 52, a programmable delay circuit 54, and a programmable pattern generator 56. The indicating signal D is applied to a data input (DI) of FIFO buffer 52 while the timing signal TD is applied to a shift-in (SI) input of FIFO buffer 52. In response to each pulse of the timing signal TD, FIFO buffer 52 stores a control bit representing the current state of indicating signal D. Programmable delay circuit 54 delays the timing signal TD with a delay determined by delay data (DELAY) produced by pattern generator 56, thereby to provide a delayed timing signal TD' to a shift-out (SO) input of FIFO buffer 52. Pattern generator 56 sets the DELAY data value provided to delay circuit 54 after each pulse of timing signal TD in accordance with a pattern defined by programming data provided as input to pattern generator 56 via computer bus 16. In response to each pulse of delayed timing signal TD', FIFO buffer 52 shifts its longest stored control bit onto a data-out terminal (DO) as the DRIVE signal provided to drive circuit 40 of FIG. 4 (fig. 4, 6, col. 6, lines 32-51, Dinteman). Thus programmable delay circuit provides a delayed timing signal TD', which is used to output signal from the buffer.

14. The applicant contends, "As per claim 23, 24 and 30, the output of Dinteman's programmable delay circuit is a timing signal TD' and not a test signal, one of skill in the art would not be motivated to modify Dinteman's test circuit in this manner."
The examiner disagrees and contends that Speyer et al. teach phase discriminator 215 and test circuit 205 function as a ring oscillator in which the period of oscillation is determined by the signal propagation

delay (col. 4, lines 42-45, Speyer et al.). Dinteman teaches a programmable delay circuit (fig. 6, Dinteman).

The applicant also contends, "Dinteman does not teach the proper data values for the pattern generator are determined experimentally."

The examiner disagrees and contends that Dinteman teaches that programmable delay circuit delays the timing signal TD with a delay determined by delay data produced by pattern generator (col. 6, lines 39-42, Dinteman).

15. The applicant contends, "As per claims 25 and 29, one of skill in the art would not be motivated to use Churchill's programmable delay circuit to produce a jittery test signal for use in jitter testing because the scan bus could not supply data to frequency modulate input signal at a sufficient rate during a test when the IC is processing the jittery test signal."

The examiner disagrees and would like to mention that Dinteman teaches programmable delay circuit (fig. 6, Dinteman). Churchill only teaches that a programmable delay circuit can be within the IC (fig. 3, col. 20, lines 28-31, Churchill et al.).

16. The applicant contends, "As per claim 26, one of skill in the art would not be motivated to embed Dinteman's pattern generator in the IC under test since it would render Dinteman's test circuit non-functional."

The examiner disagrees and would like to point out that Adams et al. teaches an ABIST circuit on an integrated circuit including a programmable pattern generator (fig. 1, col. 3, lines 31-33, Adams et al.).

17. The applicant contends, "As per claims 31, 34 and 35, one of skill in the art would not be motivated to use Churchill's programmable delay circuit to produce a jittery test signal for use in jitter testing because the scan bus could not supply data to frequency modulate input signal at a sufficient rate during a test when the IC is processing the jittery test signal."

The examiner disagrees and would like to mention that Dinteman teaches programmable delay circuit (fig. 6, Dinteman). Churchill only teaches that a programmable delay circuit can be within the IC (fig. 3, col. 20, lines 28-31, Churchill et al.).

The applicant contends, "Osawa provides no motivation for one of skill in the art to use Osawa's selector in connection with Dinteman's jitter generator circuit."

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Dinteman teaches that in decoding the incoming VECTOR, decoder 62 signals a set of four multiplexers 76 (fig. 8, col. 7, lines 28-29, Dinteman). Osawa et al. teaches selector circuit 233 (fig. 1, col. 33, lines 57-67, Osawa et al.). Thus Dinteman provides motivation to use Osawa's selector in connection with Dinteman's jitter generator circuit.

The applicant contends, "The selector cited in Chetlur does not feed back the test signal output of a programmable delay circuit to the delay circuit's input to cause the test signal to oscillate."

The examiner disagrees and would like to point out that Chetlur et al. teach a tester comprising a voltage controlled oscillator for generating a controllable frequency oscillating test signal (col. 6, lines 14-15, Chetlur et al.). Chetlur et al. also teach that the multiplexer supplies the test signal as the first signal input (fig. 1, col. 6, lines 22-24, Chetlur et al.).

Dinteman teaches a delay circuit (fig. 6, Dinteman). Dinteman also teaches that driver circuit 40 can produce a TEST signal that is a phase modulated version of the TEST signal defined by the input VECTOR data sequence, with the nature of the phase modulation being determined by the programming data inputs to event phase modulators 46 and 48 (col. 5, lines 51-56, Dinteman).

The applicant contends, "The output of Dinteman's programmable delay circuit is a timing signal TD' and not a test signal, one of skill in the art would not be motivated to modify Dinteman's test circuit."

The examiner disagrees. Dinteman teaches that the programmable delay circuit provides a delayed timing signal TD' to a shift-out input of FIFO buffer 52 (FIG. 6, col. 6, lines 39-43, Dinteman). The circuit in FIG. 6 (Dinteman) can be modified with Speyer's reference.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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